

Model, Analyze, And Simulate $\Sigma\Delta$ Fractional-N Frequency Synthesizers

Linear and nonlinear analysis techniques have been applied to the study of several fractional-N frequency-synthesizer architectures.

Part 1 of
2 parts

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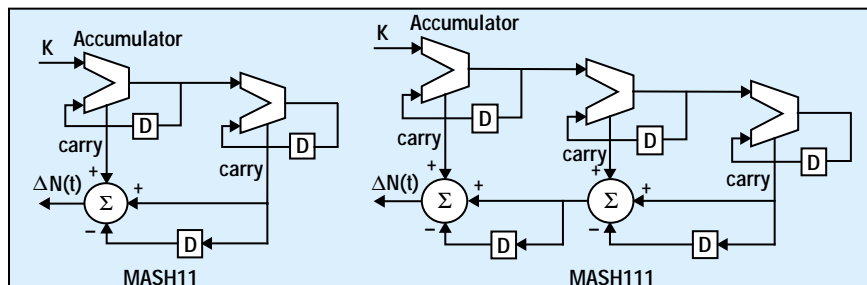
NOISE and speed are critical performance parameters for frequency synthesizers in communications systems. One of the more versatile synthesizer architectures is the $\Sigma\Delta$ fractional-N circuit, which combines fast-switching speed, high resolution, and low phase noise. But to better understand how to apply such sources, techniques were developed at Philips Semiconductors (San Jose, CA) for the analysis and synthesis of $\Sigma\Delta$ fractional-N synthesizers. Work was applied to various synthesizer configurations (MASH1, MASH11, and MASH111), and a set of mathematical expressions were developed to show the relation between the $\Sigma\Delta$ sequence and $\Sigma\Delta$ phase noise. Through analysis and simulation, it will be shown that the inherent nonlinearity of the voltage-controlled oscillator (VCO) in a fractional-N synthesizer, in conjunction with insufficiently suppressed $\Sigma\Delta$ phase noise from the synthesizer, are causes of spurious generation in the synthesizer. In addition, gain mismatch of the charge pumps and other nonlinearities inside the synthesizer loop are major contributors to the phase-noise and spurious performance of a fractional-N frequency synthesizer.

Due to the rapid growth of communications applications worldwide, system designers require frequency synthesizers with faster switching speeds and improved spurious/phase-noise performance, along with fine-grained resolution (channel

spacing). In an integer-N (or low-modulus fractional-N) frequency synthesizer, one must compromise the noise performance in order to obtain a higher switching speed, and vice versa. However, for a $\Sigma\Delta$ fractional-N frequency synthesizer, such

a trade-off does not appear to be necessary. Since an RF divider can only divide a complete number of VCO cycles, a fractional dividing ratio must be realized by means of time averaging. The multistage-noise-shaping (MASH) structure is popular within the synthesizer-design community not only because it is simple to implement in hardware, but also because it has an attractive noise-transfer function and is unconditionally stable across the full fractional region.

Figure 1 shows two MASH structures (MASH11 and MASH111) where common digital blocks such as accumulators, adders, and D flip flops are used. To begin the analysis of a $\Sigma\Delta$ frequency synthesizer, it may help to review a basic block diagram (Fig. 2). The charge pump is assumed. The block diagram is almost identical to an integer-N synthesizer, except that the dividing number $N(t)$ is varying according to the output of the $\Sigma\Delta$ calculator. The dividing number $N(t)$ consists of two parts—the constant integer N and the time-varying integer $\Delta N(t)$, which is updated by the $\Sigma\Delta$ calculator between two divisions. Parameter $\Delta N(t)$ is a periodic number and its period is twice the accumulator's overflow value. Once the hardware of the calculator is specified, $\Delta N(t)$ is the function of the integer K . The average fractional dividing ratio is equal to the K value scaled by the overflow value. The states of the $\Sigma\Delta$ calculator is updated by the edges of the RF divider output. Therefore, the updates of the $\Sigma\Delta$ calculator are not in syn-



1. The MASH11 (left) and MASH111 (right) fractional-N frequency synthesizers can be implemented with these hardware configurations.

chronization with the reference clock edges. The integer range of $\Delta N(t)$ depends on a particular $\Sigma\Delta$ modulation used by the $\Sigma\Delta$ calculator. Parameter $\Delta N(t)$ will have four levels from -1 to +2, and eight levels from -3 to +4 for the MASH11 and MASH111 configurations, respectively.

For a $\Sigma\Delta$ fractional-N frequency synthesizer, a phase error almost al-

ways exists at every compare instance. In the locked condition, the average phase error over a complete $\Sigma\Delta$ sequence, i.e., $\Delta N(t)$, must be zero. Due to the varying dividing number, the pulse edges of the RF divider output are position-modulated. When the divider output is edge-compared with the reference clock at the phase detector's input, the phase detector will

generate a phase-error (or noise) waveform which is pulse-position and pulse-width modulated. The pulse width indicates the sign and magnitude of the phase error and the pulse position indicates when this phase error occurs within a period. It is intuitive that this phase error will modulate the VCO through the charge pump/loop filter and the VCO output influences the RF divider output. Due to this "chicken and egg" dilemma, this intuition leads to a difficult situation for analyzing the synthesizer performance. Further analysis shows that among all noise sources, the phase error at the phase detector is primarily contributed by the $\Sigma\Delta$ sequence. Therefore, the analytical model for the noise/spurious performance can be abstracted into a somewhat-modified block diagram (Fig. 3), where the phase error, due to the $\Sigma\Delta$ sequence, is taken out of the loop and treated as if it came from an independent noise source at the phase detector. In this model, $N + n$ is the average dividing ratio, and n is the average fractional part.

Since the focus here is on the $\Sigma\Delta$ phase noise, other noise sources, such as those from the reference clock or the VCO itself, are not considered here. When the noise sources are not correlated, they additively contribute to the overall noise and spurious performance, and can be straightforwardly analyzed. Unlike the classic linear approach, the VCO block is split into two blocks—the VCO phase block and the sinusoidal block in this model. The feedback path starts at the VCO phase output. From the phase-feedback point of view, this point is the same as the VCO output used in hardware.

To quantify the $\Sigma\Delta$ phase-noise source in Fig. 3, two properties are used—the periodic $\Sigma\Delta$ sequence and the negligible VCO noise to the input of the phase detector. The second property enables the use of an ideal carrier with a proper frequency in calculating the $\Sigma\Delta$ phase-noise source (Fig. 4). The first property enables the expansion of the $\Sigma\Delta$ phase error at the phase-detector output, $PE(t)$, by the Fourier series:

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$$PE(t) = \sum_{i=1}^{\omega} \left[x(i) \cos(i\omega_0 t) + y(i) \sin(i\omega_0 t) \right] \quad (1)$$

$$x(i) = \sum_{j=i}^L \left(\frac{2}{\pi i} \right) \sin \left\{ \frac{i \omega_0 P_w(j)}{2} \right\} \cos \left[i \omega_0 P_p(j) \right] \quad (2)$$

$$y(i) = \sum_{j=i}^L \left(\frac{2}{\pi i} \right) \sin \left\{ \frac{i \omega_0 P_w(j)}{2} \right\} \sin \left[i \omega_0 P_p(j) \right] \quad (3)$$

where:

$P_p(i)$ = the pulse position at the i th reference clock instance (the pulse position is defined as the middle of each pulse),

$P_w(i)$ = the pulse width at the i th reference clock instance,

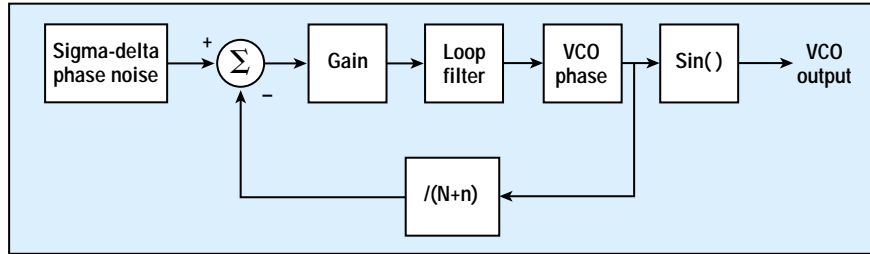
I_s = the fundamental frequency of PE(t), and

L = the length of the $\Sigma\Delta$ sequence.

The pulse width can be calculated from:

$$P_w(i) = T_c \left[\sum_{j=1}^i \Delta N(j) - in \right] \quad (4)$$

The pulse width and position are re-



3. This block diagram of a $\Sigma\Delta$ fractional-N frequency synthesizer has been modified for analysis purposes.

lated according to Eq. 5:

$$P_p(i) = T_c \left[iN + \sum_{j=1}^i \Delta N(j) \right] - \frac{[P_w(i)]}{2} = T_c iNn + \frac{P_w(i)}{2} \quad (5)$$

where:

T_c = the period of the carrier.

After eliminating $P_p(i)$ from Eqs. 2 and 3, the result is:

$$\frac{1}{\pi i} \left\{ \begin{array}{l} \sin \left[i \omega_0 P_w(j) \right] \\ \cos \left[\frac{2\pi}{L} ij \right] + \\ \left(1 - \cos \left[i \omega_0 P_w(j) \right] \right) \\ \sin \left[\frac{2\pi}{L} ij \right] \end{array} \right\} \quad (6)$$

$$y(i) = \sum_{j=1}^L \frac{1}{\pi i} \left\{ \begin{array}{l} \sin \left[i \omega_0 P_w(j) \right] \\ \cos \left[\frac{2\pi}{L} ij \right] + \\ \left(1 - \cos \left[i \omega_0 P_w(j) \right] \right) \\ \sin \left[\frac{2\pi}{L} ij \right] \end{array} \right\} \quad (7)$$

The i th harmonic power of the $\Sigma\Delta$ phase noise is then POW(i):

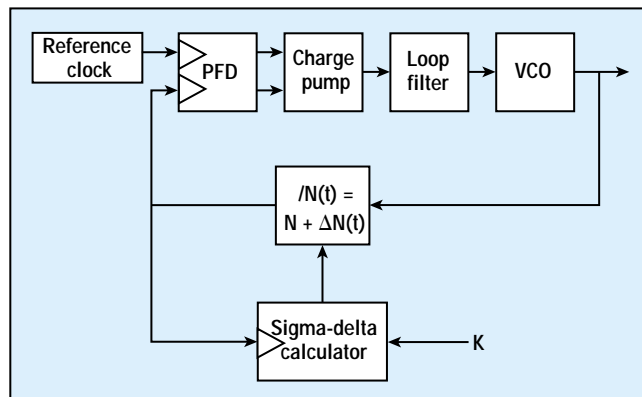
$$POW(i) = \frac{[x(i)]^2 + [y(i)]^2}{2} \quad (8)$$

Therefore, Eqs. 6, 7, and 8 establish a link between the phase error at the output of the phase detector in the time domain and the phase-noise power in the frequency domain. When $i\omega_0 P_w(j) \ll 2\pi$, $\sin[i\omega_0 P_w(j)] = i\omega_0 P_w(j)$ and $\cos[i\omega_0 P_w(j)] = 1$. Note that if $i < L/2$, that is, if it is half the reference frequency, these conditions are easily satisfied. Under this condition, Eqs. 6 and 7 become:

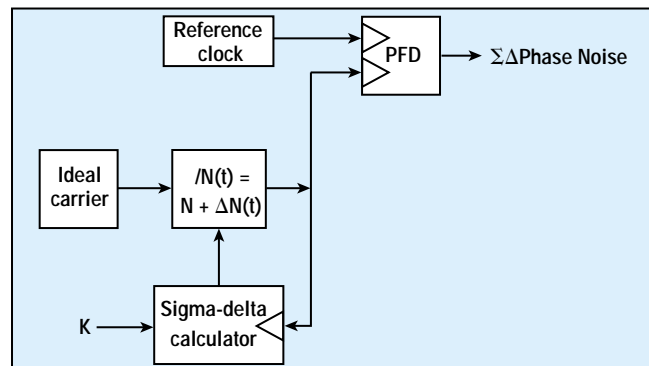
$$x(i) = \frac{\omega_0}{\pi} \sum_{j=1}^L P_w(j) \cos \left[\frac{2\pi}{L} ij \right] \quad (9)$$

$$y(i) = \frac{\omega_0}{\pi} \sum_{j=1}^L P_w(j) \sin \left[\frac{2\pi}{L} ij \right] \quad (10)$$

Equations 9 and 10 are simply the discrete Fourier transfer pair of the



2. This basic block diagram shows the structure of a $\Sigma\Delta$ fractional-N frequency synthesizer.



4. This block diagram of a $\Sigma\Delta$ fractional-N frequency synthesizer has been modified to help in calculating phase noise.

Frequency Synthesizers

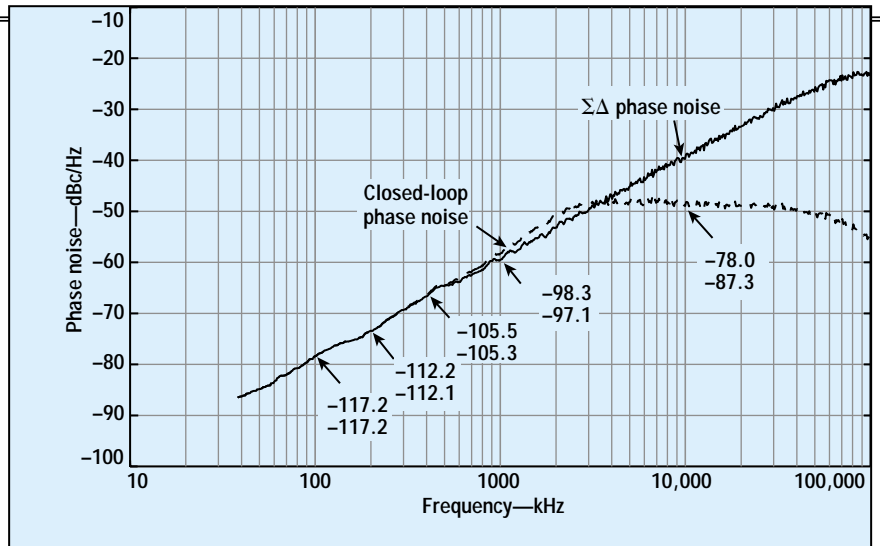
periodic phase error with a scale factor. This is why it is possible to use the FFT of the $\Sigma\Delta$ sequence to estimate the noise performance, because the AC relationship between the $\Sigma\Delta$ phase error and the $\Sigma\Delta$ sequence is an integration. Nevertheless, Eqs. 6 and 7 have an advantage in that they make it possible to explore the frequencies at higher than one-half of the reference frequency, such as the clock harmonics.

To analyze the closed-loop phase noise due to the $\Sigma\Delta$ phase noise, the classic linear approach or a novel nonlinear approach can be used. These approaches result in quite different noise/spurious performance levels. The closed-loop phase noise (or the $\Sigma\Delta$ phase noise with loop) is obtained by overlaying the closed-loop transfer function to the $\Sigma\Delta$ phase noise. The reason for this approach is that when the VCO phase noise is low, the phase modulation can be approximated by the double-sideband (DSB) amplitude modulation of as seen from:

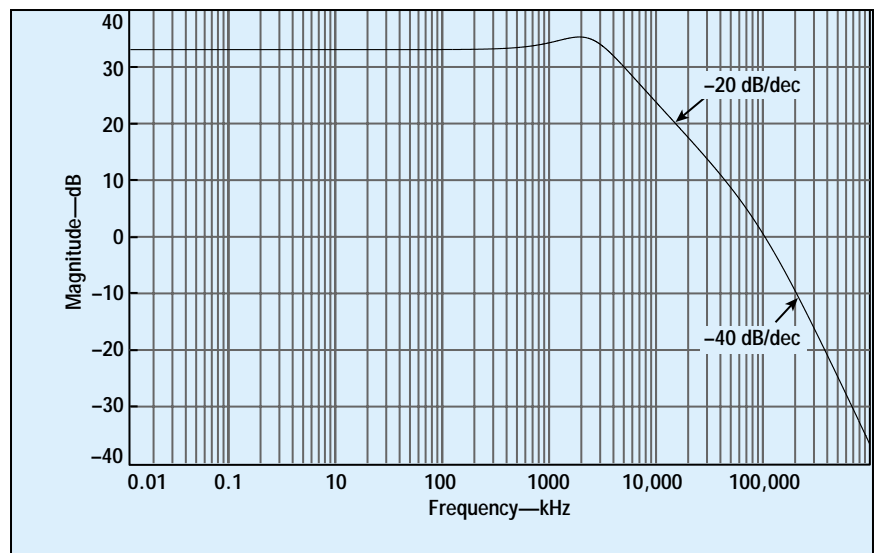
$$\begin{aligned} \cos[\omega_c t + \phi(t)] &= \cos[\phi(t)] \\ \cos(\omega_c t) - \sin[\phi(t)] \sin(\omega_c t) \end{aligned} \quad (11)$$

$$\begin{aligned} \cos[\omega_c t + \phi(t)] &= \cos(\omega_c t) \\ &\quad -\phi(t) \sin(\omega_c t) \end{aligned} \quad (12)$$

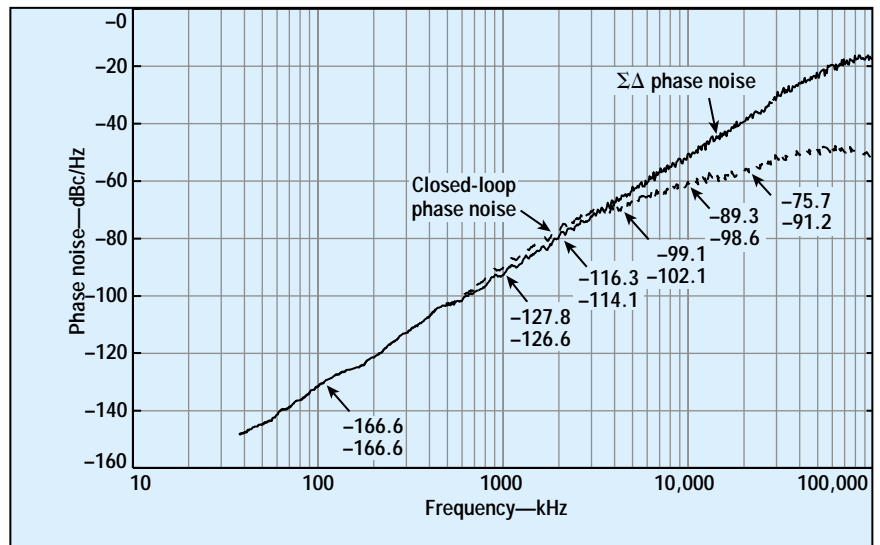
Figure 5 plots the closed-loop phase-noise spectrum (the dashed line) along with the $\Sigma\Delta$ phase-noise spectrum (the solid line) using the linear approach. The closed-loop transfer function, which incorporates a two-pole filter, is shown in Fig. 6. The spectrum was measured with a spectrum-analyzer resolution bandwidth of 7.6 kHz. MASH11 is used and K corresponds with a fractional frequency of 60 kHz with a 20-MHz reference frequency. The horizontal axis corresponds with the offset frequency from a 900.060 MHz carrier. Below 200 kHz, the $\Sigma\Delta$ phase noise and the closed-loop noise are the same; they increase with frequency at a rate of 20 dB/decade. After approximately 200 kHz, the loop filter kicks in and the slope (-20 dB/decade) of the loop transfer function cancels the $\Sigma\Delta$ phase-noise



5. This plot shows the linear closed-loop phase-noise response of a MASH11 synthesizer.



6. This plot shows the frequency response of the closed-loop transfer function for a fractional-N synthesizer, with slopes of 20 and 40 dB/decade.



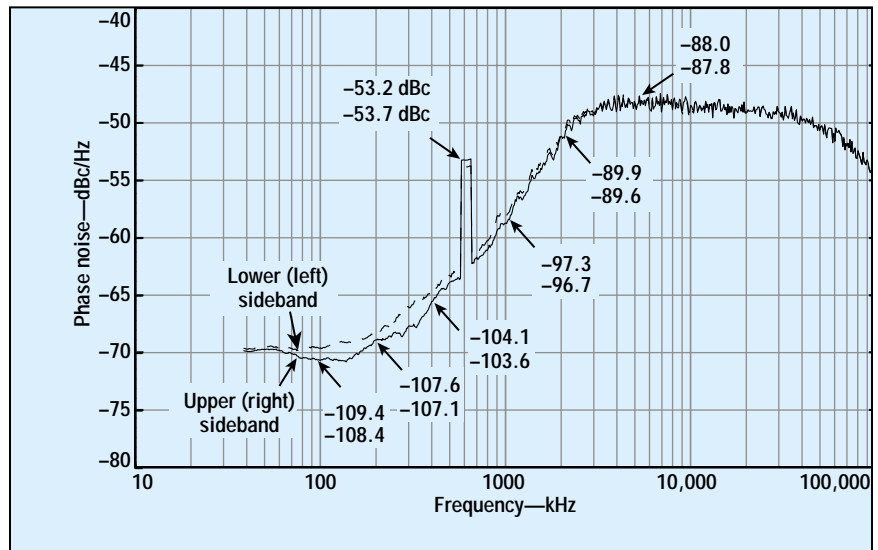
7. The linear closed-loop phase noise of a MASH11 frequency synthesizer is plotted here.

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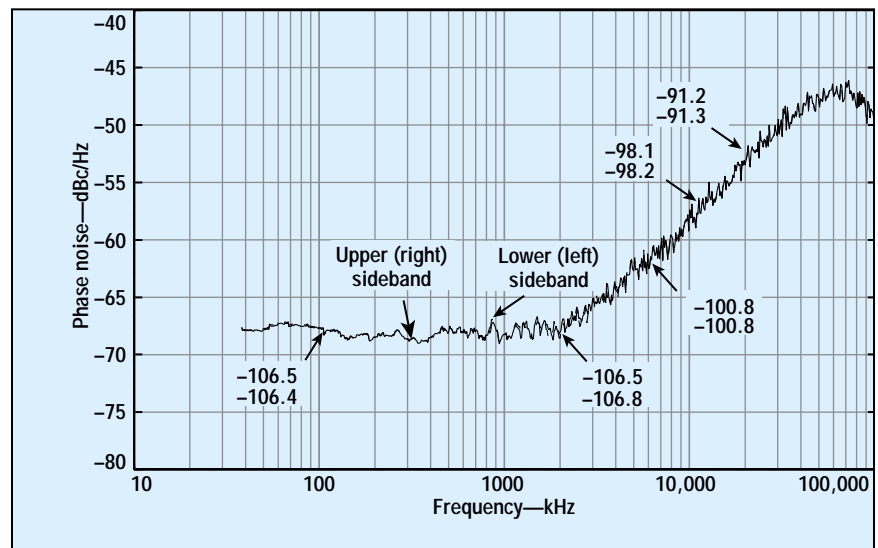
slope, which creates a flat area for the closed-loop phase noise. The close-in noise level is excellent and there is no spurious content. When the same setting is applied with the MASH111 structure, the results are somewhat different (Fig. 7). In this case, the noise slope is 40 dB/decade below 200 kHz and 20 dB/decade above 200 kHz. The close-in noise level at a 10-kHz offset for the MASH111 structure is approximately 50 dB below that for the MASH11 structure and also below the thermal-noise level.

When the $\Sigma\Delta$ phase noise is not sufficiently suppressed by the loop, the linear approach will not correctly predict the noise/spurious performance due to the inherent VCO nonlinearity (a sinusoidal function). The nonlinear approach, based on Eq. 11, better predicts the closed-loop phase noise spectrum. By using the same parameters, Figs. 8 and 9 were generated, showing the closed-loop phase-noise spectrum for the MASH11 and MASH111 structures, respectively. The upper and lower sidebands are shown in each case.

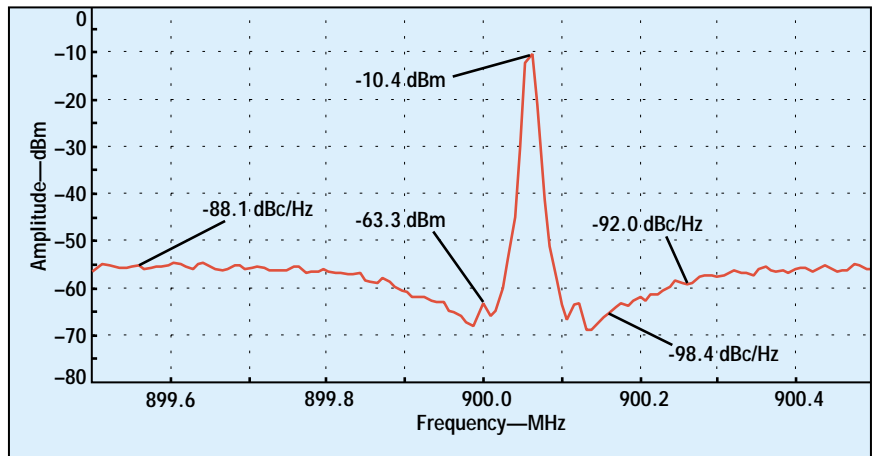
Huge differences are apparent when comparing the linear and nonlinear analysis approaches. With the MASH11 structure, there is a spur with magnitude of -53.2 dBc (in the right-hand sideband) and -53.7 dBc (in the left-hand sideband) at a frequency offset of 60 kHz, with a knee occurring at an offset frequency of approximately 10 kHz. Below the knee, the phase noise remains flat at approximately -108 dBc/Hz instead of having a slope of 20 dB/decade. Compared to Fig. 5, the close-in noise performance degradation at 10 kHz is approximately 9 dB. For offset frequencies above 100 kHz, the linear and nonlinear analyses produce similar results. With the results for the MASH111 structure shown in Fig. 9, however, no spurious content is evident. However, the knee frequency is higher than that of the MASH11 structure, at an offset frequency of approximately 2 MHz. Compared to Fig. 7, the noise performance loss at a 10-kHz offset is 60 dB. The close-in noise at a 10-kHz offset with the MASH111 structure is approximately 3 dB above that with



8. The nonlinear closed-loop phase noise of a MASH11 frequency synthesizer is plotted here.



9. The nonlinear closed-loop phase noise of a MASH111 frequency synthesizer is plotted here.



10. This plot shows the carrier spectrum of an ideal model for a MASH11 fractional-N frequency synthesizer.

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Table 1: Comparing simulations and analysis (Figs. 8 and 10)

Phase noises	Analysis	Simulation	Spurs	Analysis	Simulation
at 100 kHz	-97.3 dBc/Hz	-98.4 dBc/Hz	At 60 kHz	-53.7 dBc	-52.9 dBc
at 200 kHz	-89.9 dBc/Hz	-92.0 dBc/Hz			
at 500 kHz	-88.0 dBc/Hz	-88.1 dBc/Hz			
at 5 MHz	-89.9 dBc/Hz	-91.1 dBc/Hz			
at 10 MHz	-94.9 dBc/Hz	-96.1 dBc/Hz			

MASH11 when analyzed with the nonlinear approach. Therefore, nonlinear analysis applied to a perfect circuit configuration suggests that the MASH11 structure may not outperform MASH11 in close-in noise performance.

Generally speaking, idle tones or spurious signals appear when the phase noise is correlated. However, only when such a correlation interacts with the inherent VCO nonlinearity or other nonlinearities, can spurious generation occur. For the MASH11 structure, the spurious lo-

cation is proportional to the fractional-dividing ratio. Thanks to noise shaping and loop-filter attenuation, a fractional-dividing ratio of approximately 0 or 1 tends to make the spurious levels obvious while they become less visible as the ratio approaches 0.5. Since the MASH11 structure has a higher noise power at high frequencies than the MASH11 structure with the same loop filter, the effect of folding back is worse for the MASH11 configuration. This is clearly evidenced with the greater knee frequency and greater degrada-

tion of the close-in noise performance. Nevertheless, the VCO nonlinear effect can be sufficiently reduced if the loop filter's bandwidth is narrow enough. When this happens, the linear and nonlinear analysis approaches produce similar results.

Simulations were performed to verify the noise-prediction approaches presented above. The simulation is functionally equivalent to a synthesizer circuit. Figure 10 shows an averaged carrier-spectrum measurement with a 7.6-kHz resolution bandwidth when the MASH11 structure is used. The VCO's nominal power is -3 dBm and only positive frequencies are counted in the measurement. A spurious level of -52.9 dBc at the 60-kHz offset is even with an ideal circuit design. This is the same spur predicted in Fig. 8 with a magnitude of -53.7 dBc, which shows a strong correlation between theory and computer simulation (see Table 1).

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